IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Zvi OR-BACH et al.	Art Unit: 2826
Appl. No. 10/730,064 Confirmation No. 2943	Examiner: Tuan N. Quach
Filed: December 9, 2003	Atty. Docket No. 38897-199163
For: METHOD FOR FABRICATION OF SEMICONDUCTOR DEVICE	Customer No. 26694 PATENT TRADEMARK OFFICE

Affidavit of Zvi Or-Bach Under 37 C.F.R. § 1.132

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

I, Zvi Or-Bach, do hereby declare the following, to the best of my knowledge and belief:

1. I am the Founder, Chairman, President, and Chief Technology Officer of eASIC Corporation (as well as former Chief Executive Officer thereof), the assignee of the present application, as well as a co-inventor of the invention claimed in the present application.

2. Both eASIC Corporation and I have been recognized at various times and by various organizations/publications for achievements in the area of semiconductor device technology, for example, by *EE Times*, Red Herring, Inc., and the International Engineering Consortium. Specifically, I was named by *EE Times*, in a special project entitled, "Great Minds, Great Ideas," as on of the "Disruptors," in an article entitled, "Zvi Or-Bach Erected the Scaffolding for the

Structured ASIC." Also, as noted on the eASIC Corporation web site, "Or-Bach has been leading innovative developments in fast-turn ASIC for over 20 years. His vision led to the invention of the first Structured ASIC architecture, the first laser-based system for 1 day semiconductor customization and to the first Programmable ASIC fabric at eASIC."

3. I am also the Founder and former Chief Executive Officer of Chip Express Corporation (now, called Chipx), a company involved in the design of semiconductor devices, and more specifically, in the area of application-specific integrated circuits (ASICs) that pioneered the "Structured ASIC." I have also held engineering management positions with Elbit Computers, Ltd., Israel, and Honeywell (Lexington, MA). I hold a bachelor's degree in electrical engineering from the Technion – Israel Institute of Technology and a master's degree in computer science from the Weizmann Institute. I am listed as a sole or joint inventor on more than thirty U.S. patents.

4. To the best of my knowledge, I am not aware of any commercial vendor offering semiconductor devices involving continuous (or "borderless," as I understand these terms to be synonymous) logic arrays. In particular, I am unaware of any structured ASICs or gate arrays, including field-programmable gate arrays (FPGAs), that are commercially available, and which utilize continuous arrays, despite the fact that the use of such arrays has been suggested in the past as a way to efficiently and cost-effectively produce such semiconductor devices.

5. A problem contributing to the lack of commercial viability of the use of continuous arrays has been the problem of scaling the input/output (I/O) capability according to the size and structure of the array. The common practice is to place I/O cells (or just "I/Os") along the periphery of the logic array. With a small array, this conventional peripheral I/O tends to occupy too much of the die area, and therefore, with continuous arrays, it would be extremely wasteful to use peripheral I/O in the repetitive logic modules that are used to form continuous arrays. Note that this shortcoming of known technology is also discussed, e.g., in the U.S. patents to Sato and Anderson et al., discussed in paragraphs [0009]-[0010] of the present specification.

6. In the past, some (e.g., Sato, Anderson et al., and Sivilotti et al.) have suggested using the same transistors used for the gates of the logic portion of the array for I/O. However, this leads to problems of interfacing a resulting device (resulting from the array) with "the outside world." That is, the logic portion typically operates at significantly lower voltages than are required to interface with other devices. Hence, this solution is impractical in that it requires the engineer designing an application incorporating the device to add additional devices (e.g., step-up devices), external to the device, to permit interfacing with other devices. This would increase the size and complexity of the overall application design and would thus defeat the purpose of incorporating I/O into the device. Additionally, the logic transistors are inadequate for the

purpose of designing modern I/Os, which generally need to meet various standards and often require complex analog design techniques.

7. The ongoing presence of proposals to use continuous arrays, accompanied by such unsuccessful and/or impractical solutions to the I/O problem reflect the recognition of a need for such a solution, to make the use of continuous arrays viable.

8. The presently-claimed invention solves this problem by using "area I/Os" – I/Os located inside the device, rather than on its periphery. By designing arrays having area I/Os, a repeating module that contains logic and I/O can be formed in an area-efficient manner, so various array sizes may be constructed from a single continuous array fabric. As a result, the use of continuous arrays to produce semiconductor devices can be made viable.

9. Therefore, the addition of area I/Os to continuous arrays meets a long-felt need in the art by solving the I/O scalability problem so as to make continuous arrays commercially viable.

10. Comparing the claimed invention to the cited prior art, it is first noted that Claims 1, 3, and 16-18 (i.e., all remaining independent claims, from which all other claims depend) claim the combination of a borderless (continuous) array with at least one area I/O. It is noted that, while none of the cited prior art discloses or suggests the use of area I/Os, Applicants are aware, as

discussed in paragraph [0012] of their specification, that area I/Os have been used in the context of other technologies (e.g., "flip-chip"). However, there has been no previous suggestion or disclosure, to my knowledge, of combining area I/Os with borderless arrays, as in the claimed invention. While Padmananabhan et al., as discussed in paragraph [0011] of the present specification, discloses an array having "micro-arrays" surrounded by I/O arrays, where the micro-arrays are interconnected to form a "composite array," this also differs from the claimed invention in that such a scheme is designed so that the final device's I/Os are at the periphery of the device. Additionally, because they are not suggested, or constructed, as area I/Os, they are effectively unused and represent significant area inefficiency. Padmananabhan et al. recognizes this inefficiency and suggests that such sites might be used in some way, for example, as drivers for internal signals (i.e., not as I/Os for the device).

Regarding the cited prior art, Shenoy et al. discloses the use of peripheral I/Os, rather than area I/Os, and although Sivilotti et al. includes disclosure of borderless arrays, it suggests using the logic gate transistors to construct peripheral I/Os (rather than using area I/Os), which as discussed above is not practical given modern I/O requirements for interfacing with other components. In short, I am not aware of any prior art suggesting the use of area I/Os to solve the I/O scalability problem discussed above.

I hereby declare that the above is true, to the best of my knowledge and belief, pursuant to the provisions of 35 U.S.C. § 25 and 18 U.S.C. § 1001.

Executed this 7 day of March, 2006

By _____
Zvi Or-Bach

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